EMIF02-SPK01F2

2-line IPAD™, EMI filter and ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.07 mm x 1.47 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging

Complies with the following standards:

- IEC 61000-4-2 level 4, on output pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-2 Level 1, on input pins:
  - 2 kV (air discharge)
  - 2 kV (contact discharge)
- MIL STD 883E - Method 3015-6 Class 3

Applications

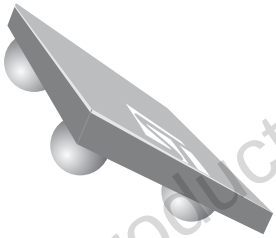
Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

Description

The EMIF02-SPK01 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 Flip-Chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up 15 kV.



Flip-Chip package (5 bumps)

Figure 1. Pin configuration (bump side)

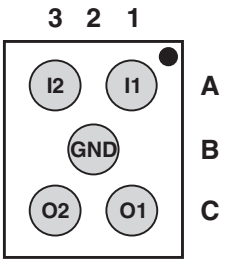
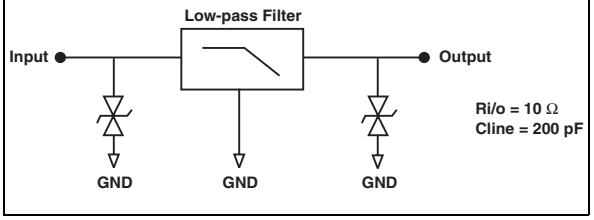


Figure 2. Basic cell configuration



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1 Electrical characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Figure 3. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage
R_D	=	Dynamic impedance
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward voltage drop
C_{line}	=	Line capacitance

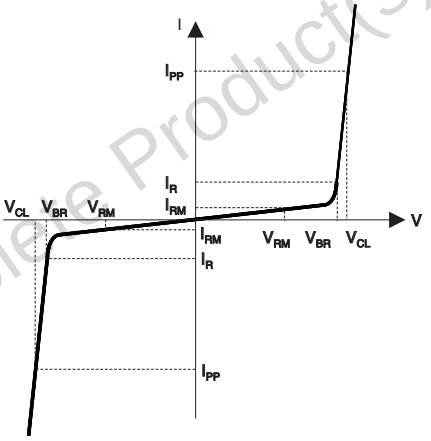

Table 2. Electrical characteristics (Tamb = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8		V
I_{RM}	V_{RM} = 3 V per line			500	nA
$R_{I/O}$	Tolerance ± 20%		10		Ω
C_{line}	V_R = 0 V		200		pF

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Figure 4. S21 (dB) attenuation measurements and Aplac simulation

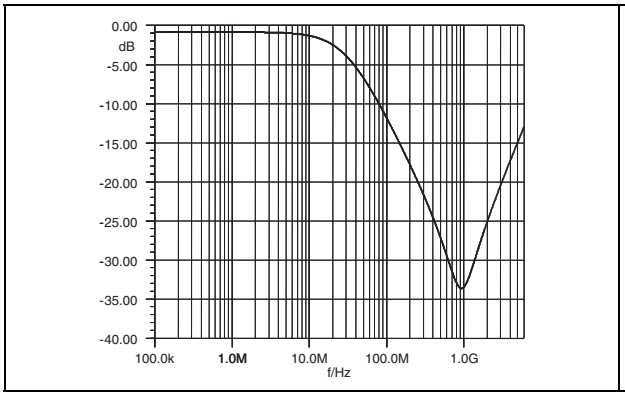

Figure 5. Analog crosstalk measurements

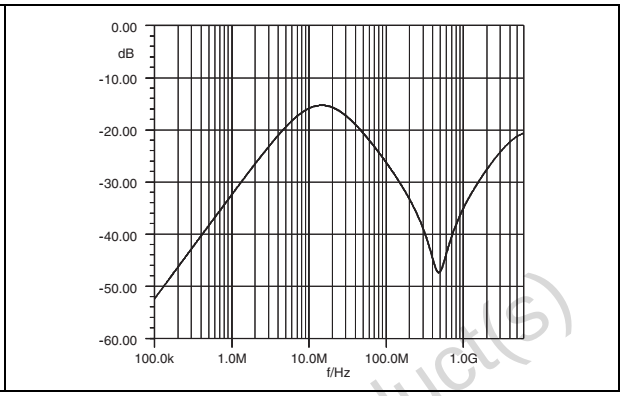

Figure 6. ESD response to IEC 61000-4-2 (+15kV air discharge) on one input $V_{(in)}$ and one output $V_{(out)}$

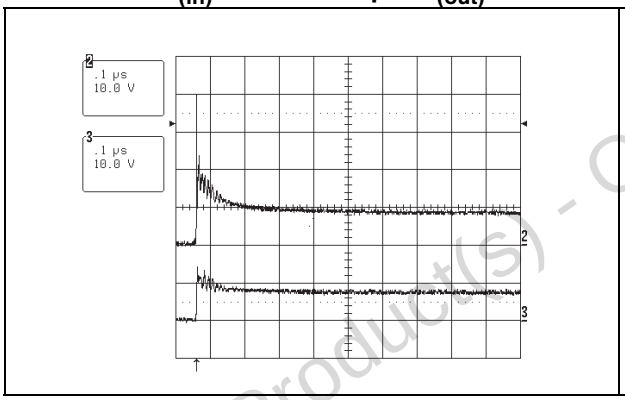

Figure 7. ESD response to IEC 61000-4-2 (–15kV air discharge) on one input $V_{(in)}$ and one output $V_{(out)}$

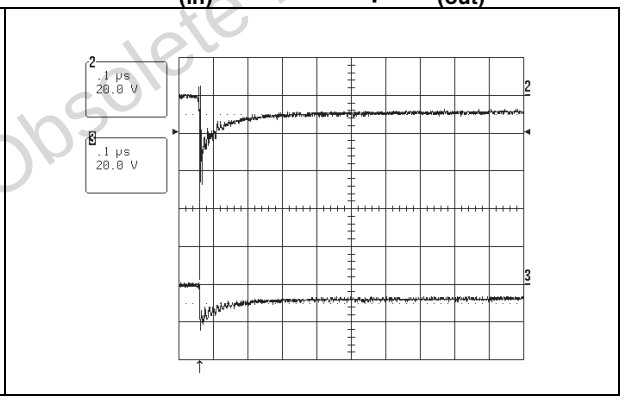

Figure 8. Line capacitance versus applied voltage

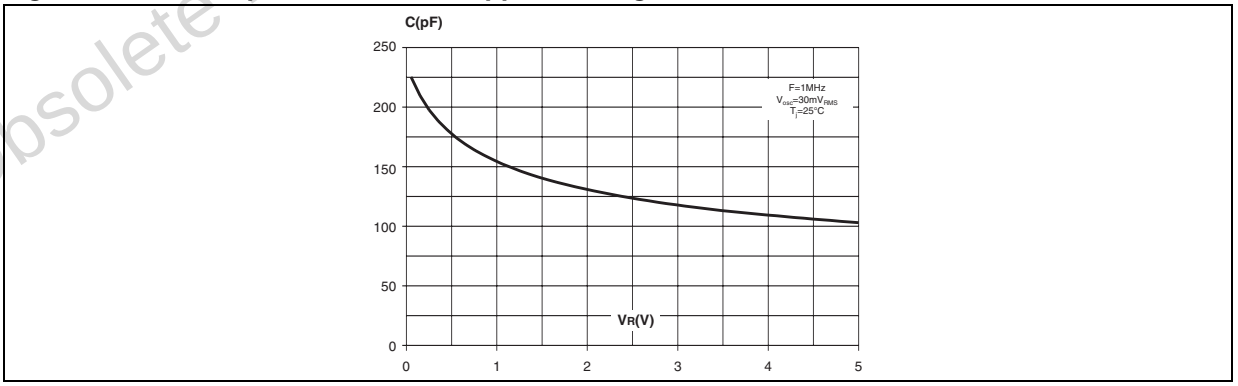

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Figure 9. Aplac mode

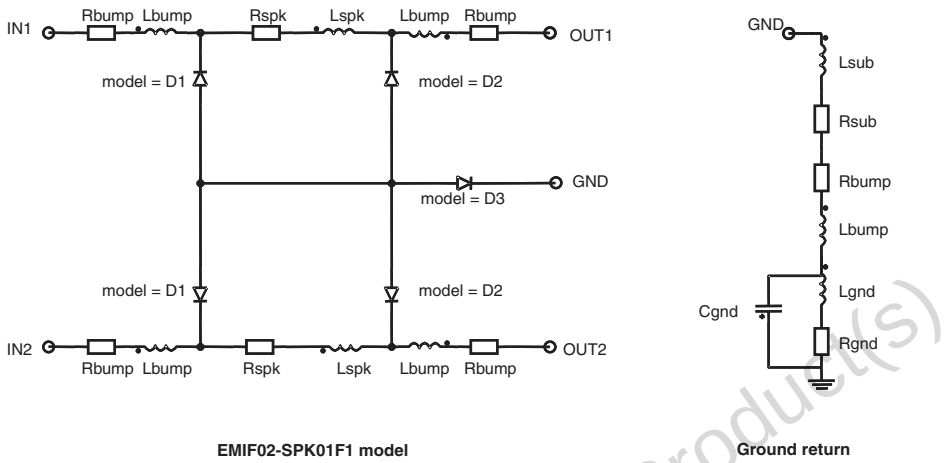

Figure 10. Aplac parameters

Model D1	Model D3	Model D2	aplacvar Ls 1nH
CJO=Cdiode1	CJO=Cdiode3	CJO=Cdiode2	aplacvar Rs 150m
BV=7	BV=7	BV=7	aplacvar Rspk 10
IBV=1u	IBV=1u	IBV=1u	aplacvar Lspk 10p
IKF=1000	IKF=1000	IKF=1000	aplacvar Cdiode1 234pF
IS=10f	IS=10f	IS=10f	aplacvar Cdiode2 3.5ppF
ISR=100p	ISR=100p	ISR=100p	aplacvar Cdiode3 1nF
N=1	N=1	N=1	aplacvar Lbump 50pH
M=0.3333	M=0.3333	M=0.3333	aplacvar Rbump 10m
RS=0.7	RS=0.12	RS=0.3	aplacvar Rsub 0.5m
VJ=0.6	VJ=0.6	VJ=0.6	aplacvar Lsub 10pH
TT=50n	TT=50n	TT=50n	aplacvar Rgnd 1m
			aplacvar Lgnd 50pH
			aplacvar Cgnd 0.15pF

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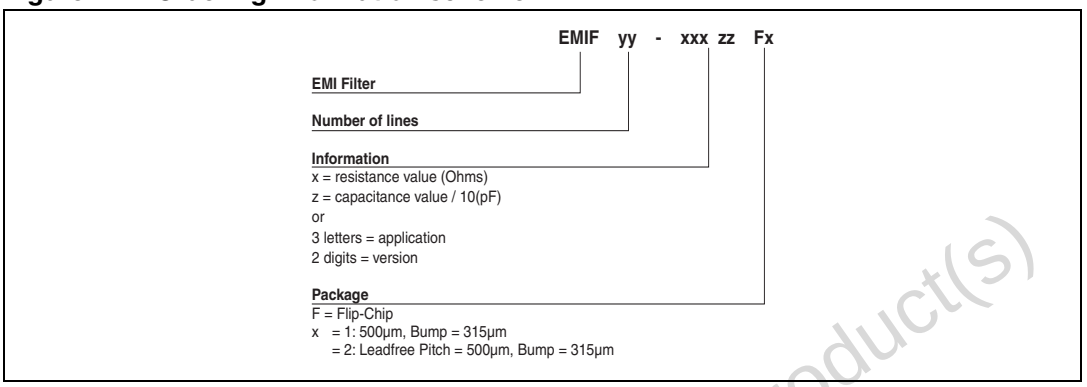
2 Ordering information

Figure 11. Ordering information scheme



3 Packaging information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 12. Flip-Chip dimensions

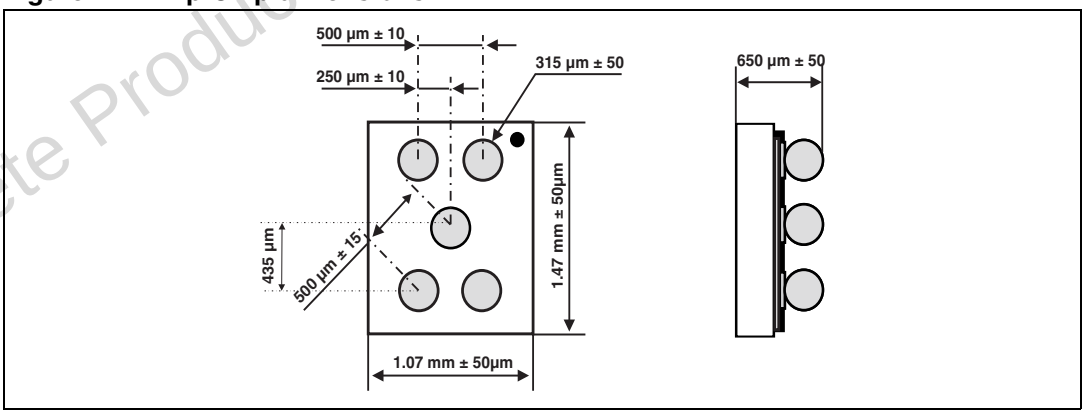


Figure 13. Footprint

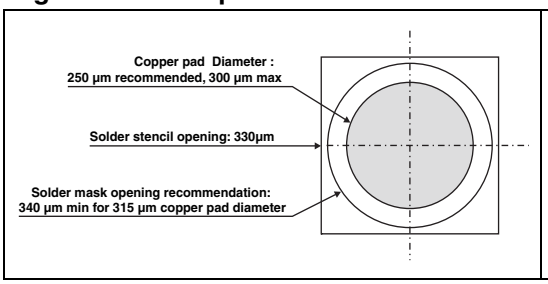


Figure 14. Marking

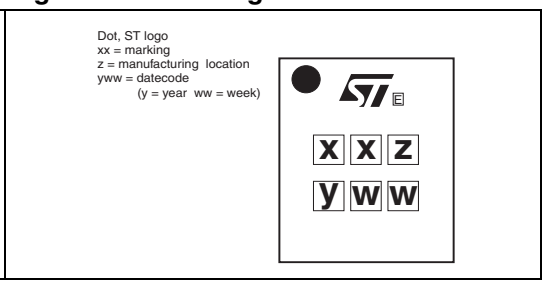


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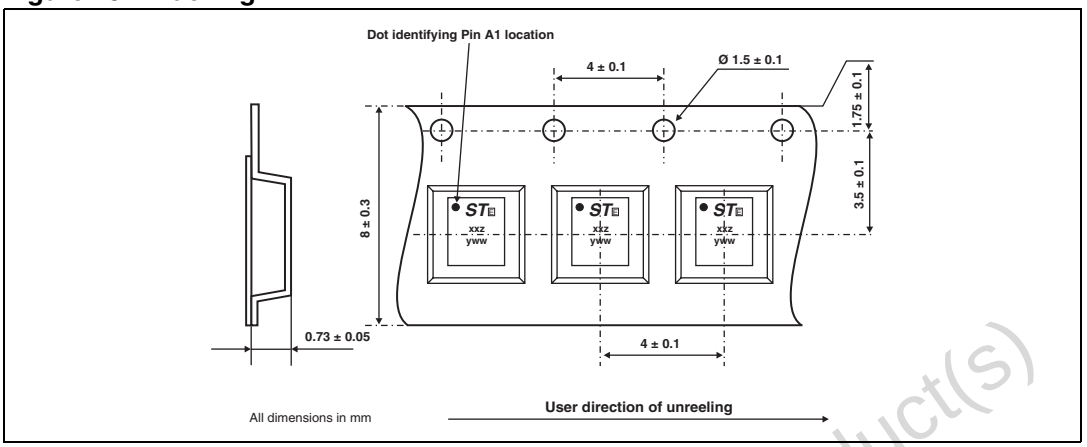
Figure 15. Packing



4 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-SPK01F2	FX	Flip Chip	2.1 mg	5000	Tape and reel (7”)

Note: More packing information is available in the applications note:
AN1235: “Flip-Chip: package description and recommendations for use”
AN 1751: “EMI filters: Recomendations and measurements”

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
14-Oct-2006	1	Initial release.
08-Sep-2011	2	Updated *Figure 12* and *Figure 13.*

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